IN THE SPECIFICATION

Please amend the paragraph beginning at page 2, line 16 to page 3, line 2, as follows:

An ECC control apparatus according to an aspect of this invention is to be connected between a host and a memory. The ECC control apparatus comprises: a first input/output circuit which inputs and outputs data to and from the host; a detecting circuit which detects a protected-data region and a redundant region of write data input to the first input/output circuit and having a predetermined data length; a code-generating circuit which generates an error correction code for correcting errors in the data stored in the protected-data region; [[an]] a code inserting circuit which inserts the error-correction code in the redundant region; and a second input/output circuit which inputs and outputs data to and from the memory.

Please amend the paragraph beginning at page 8, line 15 to page 9, line 3, as follows:

FIG. 3 is a block diagram depicting the internal structure of the ECC controller 1. The ECC controller 1 has a data-path/ECC circuit 100, an enable interface/ clock circuit 200, a control circuit 300, a counter 400, and an I/0 register 500. The data-path/ECC circuit 100 (hereinafter referred to as "DP/ECC circuit") performs a data-path process on write data and read data, generates ECD codes, corrects errors and ~~effect~~ effects some other processes. The enable interface/clock circuit 200 (hereinafter referred to as "EI/C circuit") adjusts the delay time of each enable signal, generates a clock signal and performs some other processes. The counter 400 counts the bits that constitute the write data or read data and the pulses that constitute the RE signal or WE signal. The I/O register 500 stores the data input from the host 3.

Please amend the paragraph at page 9, lines 12-24, as follows:

The bus-monitoring circuit 301 monitors the data being supplied through the buses FDH and FDN. If no data is being input or output from the ECC controller 1, no data is output to the bus FDH or the bus FDN. This is because the bus-monitoring circuit 301 generates control signals NOUTE and HOUET, which are input to the tri-state buffers 106 and 111 that are provided in the DP/ECC circuit 100. (The buffers 106 and 11 will be described later in connection with FIG. 6). Thus, the ECC controller 1 provided on the bus that connects the module 2 to the host 3 outputs no unnecessary data, preventing the host 3 and the NAND memory 2A from malfunctioning.

Please amend the paragraph beginning at page 11, line 23 to page 12, line 4, as follows:

The interruption circuit 307 makes the interruption signal active, thus effecting interruption control. The interruption circuit 307 has an error-information output circuit 308. At the same time, the interruption circuit 307 makes the interruption signal active, the error-information output circuit 308 outputs data to the host 3. The data output represents the result of the error correction that the correction circuit 114 performs as will be described later in connection with FIG. 6.

Please amend the paragraph at page 13, lines 7-23, as follows:

The WE signal input to the EI/C circuit 200 is supplied to the NAND circuit 207. The WE signal is supplied to a selector 208 and an AND circuit 221[[, too]]. The WE signal is also input to a delay circuit 205 and is delayed by a predetermine time. The WE signal thus delayed is output as a clock signal WECLK via a buffer 206. The signal output from the NAND circuit 207 is input to the selector 208. The selector 208 selects the WE signal in the

dynamic CE mode. The signal output from the selector 208 is input to a NOR circuit 209. The NOR circuit 209 receives a mask signal MSK WE output from the control circuit 300. The signal output from the NOR circuit 209 is delayed by a delay circuit 210 by a predetermined time and input to an inverter circuit 211. The inverter circuit 211 generates a signal WEo and outputs the same. The signal WEo is output as clock signal WEoCLK via a buffer 212.

Please amend the paragraph beginning at page 18, line 24 to page 19, line 10, as follows:

FIG. 7 is a diagram that represents the format of the data block used in the embodiment. In this embodiment, data is processed in units of blocks each having a predetermined number of bytes. Each data block consists of, for example, 528 bytes. Each data block is composed of a 512-byte user region and a 16-byte redundant region. A 16M-byte memory card, for example, has 32K data blocks of this type. The ECC encoding system utilizes, for example, Reed-Solomon codes and performs 4-symbol error correction (each symbol consists of 10 bits). The ECC encoding system generates an 8-symbol (80-bit) ECC code ~~is generated~~ for the 512-byte data stored in each user region. That is, the ECC code is a 10-byte code.

Please amend the paragraph at page 26, lines 16-26, as follows:

Assume that the host 3 executes the block-read command to read the read data from the NAND memory 2A. Then, the ECC controller 1 detects the block-read command on the bus FDN and starts the data-reading process. At the same time, the ECC controller 1 outputs the block-read command to the NAND memory 2A. Then, the ECC controller 1 supplies to the NAND memory 2A the address that the host 3 has output. The host 3 performs the

polling of the R/B signal and ~~start~~ starts transferring the read data from the NAND memory 2A upon detecting that the NAND memory 2A is ready.

Please amend the paragraph at page 31, lines 15-27, as follows:

How the CE-generating circuit 306 operates in the static CE mode will be explained. Assume that the ECC controller 1 controls four ~~NADND~~ NAND memories 2A to 2D. If the host 3 can allocate four chip enable (CE) signals to the NAND memories 2A to 2D, respectively, the CE-generating circuit 306 is operated in the dynamic CE mode that is the ordinary operating mode. In the dynamic CE mode, the ECC controller 1 outputs the CE[3:0] signal input from the host 3 to the NAND memory designated. In this NAND memory, the CE [3:0] signal is used as CEo [3:0] signal. Note that the CE [3:0] signal is a 4-bit signal and can control the four memories at the same time in the present embodiment.

Please amend the paragraph at page 32, lines 1-5, as follows:

The host 3 may make only one CE signal active for the NAND flash memory module 2 and only one CE signal may be allocated to the four NAND memories 2A to 2D. In this case, the ECC controller 1 operates in the static CE mode to control the four NAND memories 2A to 2D.

Please amend the paragraph at page 32, lines 13-25, as follows:

The page-data program period of the NAND memory 2A (i.e., the time required to write data from the data buffer to memory cells in the memory 2A,) is several milliseconds. The page-data read-busy period (i.e., the time required to write data from the memory cells to data buffer in the memory 2A) is hundreds of microseconds. If the CE signal supplied to the NAND memory 2A remains active throughout the page-data program period or the page-data

read-busy period, the host 3 cannot access any peripheral device on the host bus. The data-processing efficiency of the whole system will inevitably [[fall]] fail. To prevent this, the host 3 sets the ECC controller 1 in the static CE mode.

Please amend the paragraph at page 33, lines 16-22, as follows:

The ECC controller 1 has a circuit that masks the WEo or CE signal (4 bits) if the signal is not active in the static CE mode. Hence, the CEo signal is active only while the NAND memory 2A remains busy, irrespectively of the level of the external CE signal, but it is possible to prohibit ~~accesses~~ access to the NAND memory 2A by virtue of the REo or WE signal.

Please amend the paragraph at page 41, lines 20-23, as follows:

Further, the ECC controller 1 has the function of changing the region in which the ECC code is inserted. This makes it possible for the NAND memory 2A to ~~stored~~ store data in many types of formats.

Please amend the paragraph at page 42, lines 5-11, as follows:

The embodiment described above has an ECC controller 1, in addition to the host 3 and the NAND memory 2A. Nonetheless, the host 3 may ~~incorporates~~ incorporate the ECC controller 1. Alternatively, the NAND memory 2A may incorporate the ECC controller 1. In either case, the ECC controller 1 operates in the same manner as described above.